I Claim:

1. A method for producing a fault signal indicating a fault in a transmission of a data signal transmitted using differential signaling on a data line having two signal lines, which comprises the steps of:

comparing a first mid-level value having a potential in an area of a mid-point between a signal level on a first signal line and a signal level on a second signal line when transmitting a logic "1" with a second mid-level value formed when transmitting a logic "0"; and

generating the fault signal if a discrepancy between the first and second mid-level values exceeds a predetermined threshold value.

2. The method according to claim 1, which further comprises:

forming the fault signal when:

$$| (VP[1] + VN[1])/ 2 - (VP[0] + VN[0])/ 2 | > Q$$

is satisfied, where

VP[1] is the signal level on the first signal line when the logic "1" is transmitted, VP[0] is the signal level on the

first signal line when the logic "0" is transmitted, VN[1] is the signal level on the second signal line when the logic "1" is transmitted, VN[0] is the signal level on the second signal line when the logic "0" is transmitted, and Q is the predetermined threshold value.

3. The method according to claim 1, which further comprises tapping off the first and second mid-level values from a voltage divider connected to the first and second signal lines.

4. The method according to claim 3, which further comprises using two series ohmic resistors for forming the voltage divider.

5. The method according to claim 1, which further comprises:

sampling the first mid-level value when the logic "1" is transmitted using a sample and hold device and buffer-storing the first mid-level value as a first auxiliary measurement variable;

sampling the second mid-level value when the logic "0" is transmitted and buffer-storing the second mid-level value as a second auxiliary measurement variable; and

producing the fault signal if a distance between magnitudes of the first and second auxiliary measurement variables is greater than the predetermined threshold value.

6. The method according to claim 5, which further comprises:

transmitting logic "ones" and logic "zeros" alternately at a predetermined clock frequency via the data line using a clock; and

operating two sample and hold devices at half the predetermined clock frequency, using a first sample and hold device for determining the first auxiliary measurement variable and using a second sample and hold device for determining the second auxiliary measurement variable with the two sample and hold devices being operated in opposite senses such that they alternately sample a mid-level value between the first and second signal lines.

7. The method according to claim 6, which further comprises:

using a toggle flip-flop having an input side receiving the predetermined clock frequency to drive the two sample and hold devices;

using a first output signal from the toggle flip-flop as an auxiliary clock signal for the first sample and hold device; and

using a second output signal from the toggle flip-flop as a further auxiliary clock signal for the second sample and hold device.

8. The method according to claim 1, which further comprises storing the fault signal as a status signal indicating a fault in a shift register.

9. The method according to claim 8, which further comprises using a boundary scan register which is compatible with the IEEE Standard Test Access Port and Boundary-Scan Architecture as the shift register.

10. The method according to claim 4, which further comprises forming the two series ohmic resistors with identical resistance values.

11. An apparatus for producing a fault signal indicating a fault during a transmission of a data signal transmitted using differential signaling on a data line having a first signal line and a second signal line, the apparatus comprising:

a comparison device connected to the data line for comparing a first mid-level signal having a potential in an area of a mid-point between a signal level on the first signal level line and a signal level on the second signal line when transmitting a logic "1" with a second mid-level signal formed when transmitting a logic "0", said comparison device producing the fault signal if a discrepancy between the first and second mid-level signals being greater than a predetermined threshold value.

12. The apparatus according to claim 11, further comprising a line termination connected to the data line, said line termination serving as an input side for the apparatus and having a characteristic impedance matched to that of the data line.

13. The apparatus according to claim 11, further comprising a voltage divider electrically connected between said comparison device and the data line.

14. The apparatus according to claim 13, wherein said comparison device has at least one sample and hold device.

15. The apparatus according to claim 13, wherein said comparison device has:

a toggle flip-flop having an output and an inverted output; and

two sample and hold devices, including a first sample and hold device and a second sample and hold device, each connected to said voltage divider, each having a clock input, and producing output signals, said output of said toggle flip-flop connected to said clock input of said first sampled and hold device, and said inverted output of said toggle flip-flop connected to said clock input of said second sample and hold device.

16. The apparatus according to claim 15, wherein said comparison device has a comparator having inputs connected to and receiving the output signals from said two sample and hold devices, said comparator having an output and producing the fault signal available at said output.

17. The apparatus according to claim 11, further comprising a memory device for storing the fault signal, said memory device connected to said comparison device.

18. The apparatus according to claim 17, wherein said memory device is a shift register having multiplexers and D flip-flops connected to said multiplexers.